

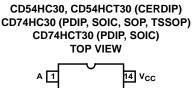
Data sheet acquired from Harris Semiconductor SCHS121D

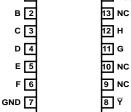
August 1997 - Revised September 2003

Features

- Buffered Inputs
- Typical Propagation Delay: 10ns at V_{CC} = 5V, $C_{L} = 15 pF, T_{A} = 25^{o}C$
- Fanout (Over Temperature Range)
 - Standard Outputs 10 LSTTL Loads
 - Bus Driver Outputs 15 LSTTL Loads
- Wide Operating Temperature Range ... -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
 - 2V to 6V Operation
 - High Noise Immunity: NIL = 30%, NIH = 30% of V_{CC} at $V_{CC} = 5V$
- HCT Types
 - 4.5V to 5.5V Operation
 - Direct LSTTL Input Logic Compatibility, $V_{II} = 0.8V$ (Max), $V_{IH} = 2V$ (Min)
 - CMOS Input Compatibility, $I_I \le 1\mu A$ at V_{OL} , V_{OH}

Pinout





CD54/74HC30, CD54/74HCT30

High Speed CMOS Logic 8-Input NAND Gate

Description

The 'HC30 and 'HCT30 each contain an 8-input NAND gate in one package. They provide the system designer with the direct implementation of the positive logic 8-input NAND function. Logic gates utilize silicon gate CMOS technology to achieve operating speeds similar to LSTTL gates with the low power consumption of standard CMOS integrated circuits. All devices have the ability to drive 10 LSTTL loads. The HCT logic family is functionally pin compatible with the standard LS logic family.

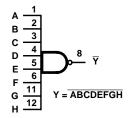
Ordering Information

PART NUMBER	TEMP. RANGE (^o C)	PACKAGE
CD54HC30F3A	-55 to 125	14 Ld CERDIP
CD54HCT30F3A	-55 to 125	14 Ld CERDIP
CD74HC30E	-55 to 125	14 Ld PDIP
CD74HC30M	-55 to 125	14 Ld SOIC
CD74HC30MT	-55 to 125	14 Ld SOIC
CD74HC30M96	-55 to 125	14 Ld SOIC
CD74HC30NSR	-55 to 125	14 Ld SOP
CD74HC30PW	-55 to 125	14 Ld TSSOP
CD74HC30PWR	-55 to 125	14 Ld TSSOP
CD74HC30PWT	-55 to 125	14 Ld TSSOP
CD74HCT30E	-55 to 125	14 Ld PDIP
CD74HCT30M	-55 to 125	14 Ld SOIC
CD74HCT30MT	-55 to 125	14 Ld SOIC
CD74HCT30M96	-55 to 125	14 Ld SOIC

NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small-quantity reel of 250.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures. Copyright © 2003, Texas Instruments Incorporated.

Functional Diagram

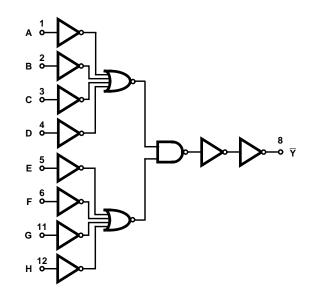


TRUTH TABLE

			INP	UTS				
Α	В	С	D	Е	F	G	н	OUTPUT
L	Х	Х	Х	Х	Х	Х	Х	Н
Х	L	Х	Х	Х	Х	Х	х	Н
Х	х	L	Х	Х	Х	Х	Х	н
Х	х	Х	L	Х	Х	Х	Х	н
Х	х	Х	Х	L	Х	Х	Х	н
Х	х	Х	Х	Х	L	Х	х	Н
Х	х	Х	Х	Х	Х	L	х	н
Х	х	Х	Х	Х	Х	Х	L	н
н	н	Н	Н	Н	Н	Н	Н	L

NOTE: H = HIGH Voltage Level, L = LOW Voltage Level, X = Irrelevant

Logic Symbol



Absolute Maximum Ratings

DC Supply Voltage, V _{CC} 0.5V to 7V DC Input Diode Current, I _{IK}
For $V_{I} < -0.5V$ or $V_{I} > V_{CC} + 0.5V$ ±20mA
DC Output Diode Current, I _{OK}
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$
DC Output Source or Sink Current per Output Pin, I _O For V _O > -0.5V or V _O < V _{CC} + 0.5V
$DC V_{CC} \text{ or Ground Current, } I_{CC \text{ or }} I_{GND} \dots \pm 50 \text{mA}$
Operating Conditions

Temperature Range (T _A)55 ^o C to 125 ^o C
Supply Voltage Range, V _{CC}
HC Types
HCT Types4.5V to 5.5V
DC Input or Output Voltage, VI, VO 0V to VCC
Input Rise and Fall Time
2V
4.5V 500ns (Max)
6V

Thermal Information

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

			ST ITIONS		25 ⁰ C			-40 ⁰ C T	0 +85 ⁰ C	-55°C TO 125°C		
PARAMETER	SYMBOL	V _I (V)	I _O (mA)	V _{CC} (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES									-		_	
High Level Input	VIH	-	-	2	1.5	-	-	1.5	-	1.5	-	V
Voltage				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input	VIL	-	-	2	-	-	0.5	-	0.5	-	0.5	V
Voltage				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	V _{OH}	V _{IH} or V _{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output	1		-	-	-	-	-	-	-	-	-	V
Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output	VOL	V _{IH} or	0.02	2	-	-	0.1	-	0.1	-	0.1	V
Voltage CMOS Loads		VIL	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output	1		-	-	-	-	-	-	-	-	-	V
Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	lı	V _{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	μA

DC Electrical Specifications (Continued)

			ST ITIONS			25 ⁰ C		-40 ⁰ C T	O +85 ⁰ C	-55°C T	O 125 ⁰ C	
PARAMETER	SYMBOL	V _I (V)	I _O (mA)	V _{CC} (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
Quiescent Device Current	Icc	V _{CC} or GND	0	6	-	-	2	-	20	-	40	μA
HCT TYPES												
High Level Input Voltage	V _{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V _{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V _{OH}	V _{IH} or V _{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V _{OL}	V _{IH} or V _{IL}	-0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	lı	V _{CC} and GND	-	5.5	-		±0.1	-	±1	-	±1	μA
Quiescent Device Current	Icc	V _{CC} or GND	0	5.5	-	-	2	-	20	-	40	μA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load (Note 2)	ΔI _{CC}	V _{CC} -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μA

NOTE:

2. For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS
All	0.6

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Specifications table, e.g. 360 μA max at 25 $^{o}C.$

Switching Specifications Input t_r , $t_f = 6ns$

		TEST	v _{cc}	25 ⁰ C			-40°C TO 85°C		-55°C TO 125°C		
PARAMETER	SYMBOL	CONDITIONS	(V)	MIN	ΤΥΡ	MAX	MIN	MAX	MIN	MAX	UNITS
HC TYPES							-		-		
Propagation Delay, Input to	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	130	-	165	-	195	ns
Output (Figure 1)			4.5	-	-	26	-	33	-	39	ns
			6	-	-	22	-	28	-	33	ns
Propagation Delay, Data Input to Output Y	t _{PLH} , t _{PHL}	C _L = 15pF	5	-	10	-	-	-	-	-	ns

		TEST	v _{cc}		25 ⁰ C		-40 ⁰ C T	О 85 ⁰ С	-55°C T	O 125 ⁰ C	
PARAMETER	SYMBOL	CONDITIONS	(Ŭ)	MIN	ТҮР	MAX	MIN	MAX	MIN	MAX	UNITS
Transition Times (Figure 1)	t _{TLH} , t _{THL}	C _L = 50pF	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Input Capacitance	CI	-	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 3, 4)	C _{PD}	-	5	-	25	-	-	-	-	-	pF
HCT TYPES											
Propagation Delay, Input to Output (Figure 2)	t _{RHL} , t _{PHL}	C _L = 50pF	4.5	-	-	28	-	35	-	42	ns
Propagation Delay, Data Input to Output Y	t _{PLH} , t _{PHL}	C _L = 15pF	5	-	11	-	-	-	-	-	ns
Transition Times (Figure 2)	t _{TLH} , t _{THL}	C _L = 50pF	4.5	-	-	15	-	19	-	22	ns
Input Capacitance	CI	-	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 3, 4)	C _{PD}	-	5	-	26	-	-	-	-	-	pF

Switching Specifications Input t_r, t_f = 6ns (Continued)

NOTES:

3. C_{PD} is used to determine the dynamic power consumption, per gate.

4. $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = Input Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

Test Circuits and Waveforms

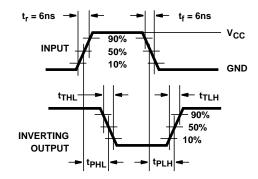


FIGURE 1. HC AND HCU TRANSITION TIMES AND PROPAGA-TION DELAY TIMES, COMBINATION LOGIC

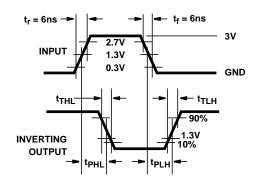


FIGURE 2. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC



10-Jun-2014

PACKAGING INFORMATION

Orderable Device	Status	Package Type		Pins	-	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
5962-8974601CA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8974601CA CD54HCT30F3A	Samples
8404001CA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	8404001CA CD54HC30F3A	Samples
CD54HC30F	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD54HC30F	Samples
CD54HC30F3A	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	8404001CA CD54HC30F3A	Samples
CD54HCT30F3A	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8974601CA CD54HCT30F3A	Samples
CD74HC30E	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC30E	Samples
CD74HC30EE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC30E	Samples
CD74HC30M	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC30M	Samples
CD74HC30M96	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC30M	Samples
CD74HC30M96G4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC30M	Samples
CD74HC30MG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC30M	Samples
CD74HC30MT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC30M	Samples
CD74HC30MTE4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC30M	Samples
CD74HC30NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC30M	Samples
CD74HC30PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ30	Samples
CD74HC30PWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ30	Samples
CD74HC30PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ30	Samples



10-Jun-2014

Orderable Device	Status	Package Type	•	Pins	•		Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
CD74HC30PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ30	Samples
CD74HC30PWT	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ30	Samples
CD74HCT30E	ACTIVE	PDIP	Ν	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT30E	Samples
CD74HCT30EE4	ACTIVE	PDIP	Ν	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT30E	Samples
CD74HCT30M	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	НСТ30М	Samples
CD74HCT30M96	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	НСТ30М	Samples
CD74HCT30MT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	НСТ30М	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.



PACKAGE OPTION ADDENDUM

10-Jun-2014

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF CD54HC30, CD54HCT30, CD74HC30, CD74HCT30 :

- Catalog: CD74HC30, CD74HCT30
- Military: CD54HC30, CD54HCT30

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

www.ti.com

TAPE AND REEL INFORMATION

REEL DIMENSIONS

Texas Instruments





TAPE AND REEL INFORMATION

TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC30M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74HC30MT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74HC30NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD74HC30PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC30PWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HCT30M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74HCT30MT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TEXAS INSTRUMENTS

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PACKAGE MATERIALS INFORMATION

14-Jul-2012



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC30M96	SOIC	D	14	2500	367.0	367.0	38.0
CD74HC30MT	SOIC	D	14	250	367.0	367.0	38.0
CD74HC30NSR	SO	NS	14	2000	367.0	367.0	38.0
CD74HC30PWR	TSSOP	PW	14	2000	367.0	367.0	35.0
CD74HC30PWT	TSSOP	PW	14	250	367.0	367.0	35.0
CD74HCT30M96	SOIC	D	14	2500	367.0	367.0	38.0
CD74HCT30MT	SOIC	D	14	250	367.0	367.0	38.0

J (R-GDIP-T**) 14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- \triangle The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.





NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



A. An integration of the information o

Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153





NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



MECHANICAL DATA

PLASTIC SMALL-OUTLINE PACKAGE

0,51 0,35 ⊕0,25⊛ 1,27 8 14 0,15 NOM 5,60 8,20 5,00 7,40 \bigcirc Gage Plane ₽ 0,25 7 1 1,05 0,55 0°-10° Δ 0,15 0,05 Seating Plane — 2,00 MAX 0,10PINS ** 14 16 20 24 DIM 10,50 10,50 12,90 15,30 A MAX A MIN 9,90 9,90 12,30 14,70 4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.

NS (R-PDSO-G**)

14-PINS SHOWN

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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